REMARKS/ARGUMENTS

Claims 5-10 are pending in this application.

Applicant appreciates the Examiner's indication that claims 7 and 10 would be allowable if rewritten in independent form including all of the features of the base claim and any intervening claims.

Claims 5, 6, 8, and 9 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mitsuda (U.S. 5,973,551). Applicant respectfully traverses the prior art rejection of claims 5, 6, 8, and 9.

Claim 5 recites:

> An overcurrent detection circuit which detects an overcurrent when the overcurrent flows to an output transistor including an input terminal to which a supply voltage is input, a control terminal to which a control voltage is input, and an output terminal from which an output current is output, the overcurrent detection circuit comprising:
>
> a monitor transistor including a control terminal and an output terminal which are connected to the control terminal and the output terminal respectively of the output transistor;
>
> **an output current detection transistor including** an input terminal to which a supply voltage is input, **a control terminal to which a detection bias voltage is input**, and an output terminal which is connected to an input terminal of the monitor transistor;
>
> a constant current source that generates a reference current;
>
> **a reference transistor including an input terminal to which a supply voltage is input, a control terminal to which the detection bias voltage is input**, and an output terminal from which the reference current flows to the constant current source; and
>
> **a comparison circuit that detects an overcurrent when the overcurrent flows to the output transistor by comparing the voltage of the output terminal of the output current detection transistor and the voltage of the output terminal of the reference transistor, and outputs an overcurrent detection signal**. (emphasis added)

With the unique combination and arrangement of method steps and features recited in Applicant's claim 5, Applicant has been able to provide a regulator that has a stable overcurrent detection level and an improved reliability (see, for example, paragraph [0016] of Applicant's Specification).

The Examiner alleged that Mitsuda teaches each and every one of the features recited in claim 5. More specifically, the Examiner alleged that "Mitsuda discloses an overcurrent detection circuit [Fig. 2] ... a reference transistor [Fig. 2; transistor Q2] including an input terminal to which a supply voltage is input, a control terminal to which the detection bias voltage is input, and an output terminal from which the reference current flows to the constant current source; and a comparison circuit [Fig. 2; comparator 2] that detects an overcurrent when the overcurrent flows to the output transistor [Fig. 2; Q1] by comparing the voltage of the output terminal of the output current detection transistor [Fig. 2; Q3] and the voltage of the output terminal of the reference transistor [Fig. 2; Q2], and outputs an overcurrent detection signal [Fig. 2; signal coming out from control circuit 1 and going to the gate terminal of the output transistor Q1; col. 4 lines 30 - col. 5 lines 62]." Applicant respectfully disagrees.

Mitsuda teaches an abnormal current detection circuit that includes an output transistor Q1, current detection transistor Q2, and a comparator circuit 2 including a third transistor Q3 and fourth transistor Q4, as shown in Fig. 2 of Mitsuda. In the third paragraph on the second page of the Outstanding Office Action, the Examiner alleged that that the output transistor Q1 includes a control terminal to which a control voltage is input, "[gate terminal of transistor Q1, which is controlled by control circuit 1]." However, the Examiner also later states in the same paragraph that the comparison circuit outputs an over-current detection signal, and that this over-current detection signal is the signal coming out from the control circuit 1 and going into the gate terminal of the output transistor Q1. Clearly, the gate terminal of the output transistor is only connected to a single input, as shown in Fig. 2 of Mitsuda. The Examiner has failed to explain how the one signal being fed into the output transistor Q1, can be *both* the control voltage and the over current detection signal, which of course it cannot.

Additionally, in the third paragraph on page 2 of the outstanding Office Action, the Examiner alleges: 1) that the drain of the output transistor Q1 is connected to a supply voltage Vcc, 2) a control terminal of the reference transistor Q2 is connected to a detection bias voltage, and 3) an input terminal of the output current detection transistor Q3 is connected to

Vcc, shown in Fig. 2 of Mitsuda. However, Fig 2 of Mitsuda clearly shows that neither Q1 nor Q3 are connected to Vcc. Furthermore, the Examiner has also failed to explain where the Mitsuda reference provides a teaching or suggestion of a detection bias voltage being input into a reference transistor.

Accordingly, Mitsuda fails to teach the features of "an output current detection transistor including ... a control terminal to which a detection bias voltage is input," "a reference transistor including an input terminal to which a supply voltage is input [and] a control terminal to which the detection bias voltage is input," and "a comparison circuit that detects an overcurrent when the overcurrent flows to the output transistor by comparing the voltage of the output terminal of the output current detection transistor and the voltage of the output terminal of the reference transistor, and outputs an overcurrent detection signal."

Thus, contrary to the Examiner's allegations, Mitsuda does not teach each and every limitation recited in claim 5. The Examiner is reminded that a "claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Accordingly, Applicant respectfully submits that Mitsuda fails to teach or suggest the unique combination and arrangement of features recited in claim 5 of the present application.

In view of the foregoing remarks, Applicant respectfully submits that claim 5 is allowable. Claims 6-10 depend upon claim 5, and are therefore allowable for at least the reasons that claim 5 is allowable.

In view of the foregoing remarks, Applicant respectfully submits that this application is in condition for allowance. Favorable consideration and prompt allowance are solicited.

To the extent necessary, Applicant petitions the Commissioner for a ONE-month extension of time, extending to December 28, 2008, the period for response to the Office Action dated August 28, 2008.

The Commissioner is authorized to charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1353.

Respectfully submitted,

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